

**Form PTO-1449** (modified)

List of Patents and Publications

For Applicant's Information

Disclosure Statement

(Use several sheets if necessary)

ATTY. DKT. NO. 5580-02102

APPLICANT: Joseph M. Ingino, Jr.

FILING DATE: July 9, 2003

SERIAL NO. 10/616,447

GROUP: Unknown

**U.S. PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
BT	B1	6,597,217	7/22/03	Ingino, Jr.	327	158	
BT	B2	6,356,158	3/12/02	Lesea	331	11	
BT	B3	6,097,227	8/1/00	Hayashi	327	158	
BT	B4	5,999,353	12/7/99	Hase, et al.	366	51	
BT	B5	4,319,207	3/9/82	Gignoux	331	173	

**FOREIGN PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**


EXAMINER:

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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
BT		5,151,665	9/29/92	Wentzler	331	8	
		5,345,119	9/6/94	Khoury	327	553	
		5,559,474	9/24/96	Matsumoto, et al.	331	17	
		5,631,587	5/20/97	Co, et al.	327	107	
		5,977,806	11/2/99	Kikuchi	327	157	
		6,127,880	10/3/00	Holst, et al.	327	531	
		5,404,250	4/4/95	Hase, et al.	360	51	
		6,037,622	3/14/00	Lin, et al.	257	299	
		6,046,626	4/4/00	Saeki, et al.	327	536	
		5,898,336	4/27/99	Yamagushi	327	157	
		6,320,470	11/20/01	Arai, et al.	331	17	
		5,512,861	4/30/96	Sharma	331	74	
		5,485,126	1/16/96	Gersbach, et al.	327	57	
		6,441,660	8/27/02	Ingino, Jr.	327	156	
		6,483,358	11/19/02	Joseph Ingino, Jr.	327	157	
		5,130,883	7/92	Edwards	361	91.1	
		3,908,159	9/75	Griffey	363	54	
BT	A1	6,566,970	5/20/02	Joseph Ingino, Jr.	331	57	

**FOREIGN PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
BT		282 673	9/21/88	EP			

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6/23/04

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**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

JS		Young, et al., "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, 9 pages.
		Vincent R. von Kaenel, "A High-Speed, Low-Power Clock Generator for a Microprocessor Application," IEEE Journal of Solid-State Circuits, Vol. 33, NO. 11, November 1998, 3 pages.
		Patrik Larsson, Bell Labs, Lucent Technologies, Holmdel, NJ, "A2-1600MHz 1.2-2.5V CMOS Clock-Recovery PLL with Feedback Phase-Selection and Averaging Phase-Interpolation for Jitter Reduction," IEEE International Solid-State Circuits Conference, ISSCC99/Session 20/Paper WA 20.6, 1999, 1 page.
		Bult, et al., "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain," IEEE Journal of Solid-State Circuits, Vol. 25, NO. 6, December 1990, 3 pages.
		von Kaenel, et al., "A 320 MHz, 1.5 mW @ 1.35 V CMOS PLL for Microprocessor Clock Generation," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, 4 pages.
		Horowitz, "The Art of Electronics," Cambridge Univ. Press, 198015 pages.
		SiByte, "Target Applications," <a href="http://sibyte.com/mercurian/applications.htm">http://sibyte.com/mercurian/applications.htm</a> , January 15, 2001, 2 pages.
		SiByte, "SiByte Technology," <a href="http://sibyte.com/mercurian/technology.htm">http://sibyte.com/mercurian/technology.htm</a> , January 15, 2001, 3 pages.
		SiByte, "The Mercurian Processor," <a href="http://sibyte.com/mercurian">http://sibyte.com/mercurian</a> , January 15, 2001, 2 pages.
		SiByte, "Fact Sheet," SB-1 CPU, October 2000, rev. 0.1, 1 page.
		SiByte, "Fact Sheet," SB-1250, October 2000, rev. 0.2, 10 pages.
		Stepanian, SiByte, "SiByte SB-1 MIPS64 CPU Core, Embedded Processor Forum 2000, June 13, 2000, 15 pages.
		Jim Keller, "The Mercurian Processor: A High Performance, Power-Efficient CMP for Networking," October 10, 2000, 22 pages.
JS		Tom R. Halfhill, "SiByte Reveals 64-Bit Core For NPUs; Independent MIPS64 Design Combines Low Power, High Performance," Microdesign Resources, June 2000, Microprocessor Report, 4 pages.

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